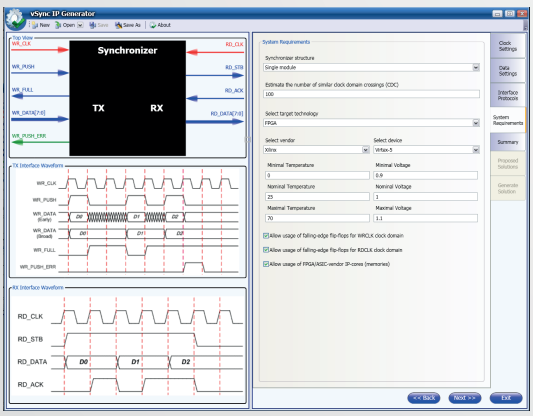
VSYNC circuits

Vincent Platform

A Complete Solution for Multiple-Clock Domain SoC Integration and Verification

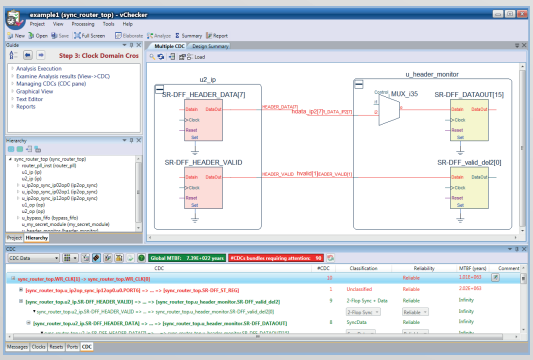
vGenerator



The vGenerator EDA tool generates and customizes reliable synchronization solutions for each interface and clock domain crossing

- Guides the user through the requirement specification
- Supports different interface protocols
- Generates multiple reliable synchronization solutions and suggests the preferred one
- Generates simulation models for the chosen solution
- Generates synthesis and P&R constraints
- Contains rich IP data base with different synchronization solutions: Point-to-point, NoC, Reset synchronization, Clock gating and switching, Static crossings
- Supports different operating conditions
- Supports multiple FPGA design flows: Xilinx, Altera, Actel, Lattice
- Supports multiple ASIC design flows: Synopsys, Cadence
- Can be tuned for a specific ASIC technology

vChecker



The vChecker EDA tool analyzes a design for synchronization failures

- Applied at Register Transfer Level (RTL) and/or at Gate Level (GL)
- Supports VHDL, Verilog and SystemVerilog
- Guides the user through the entire analysis process
- Identifies clock domain crossings statically without simulation
- Classifies clock domain crossing into correctly and incorrectly synchronized crossings
- Identifies custom synchronizers
- Identifies and verifies Vendor (Xilinx/Altera/Synopsys) synchronizers
- Identifies synchronizers generated by vGenerator
- Identifies and verifies asynchronous resets
- Grades design reliability
- Suggests correct solutions for identified incorrect clock domain crossings (a link to vGenerator)
- Generates synthesis and P&R constraints
  Supports different operating conditions
- Has a graphical interface for clock domain crossing exploration
- Directly links to the RTL code through built in text editor

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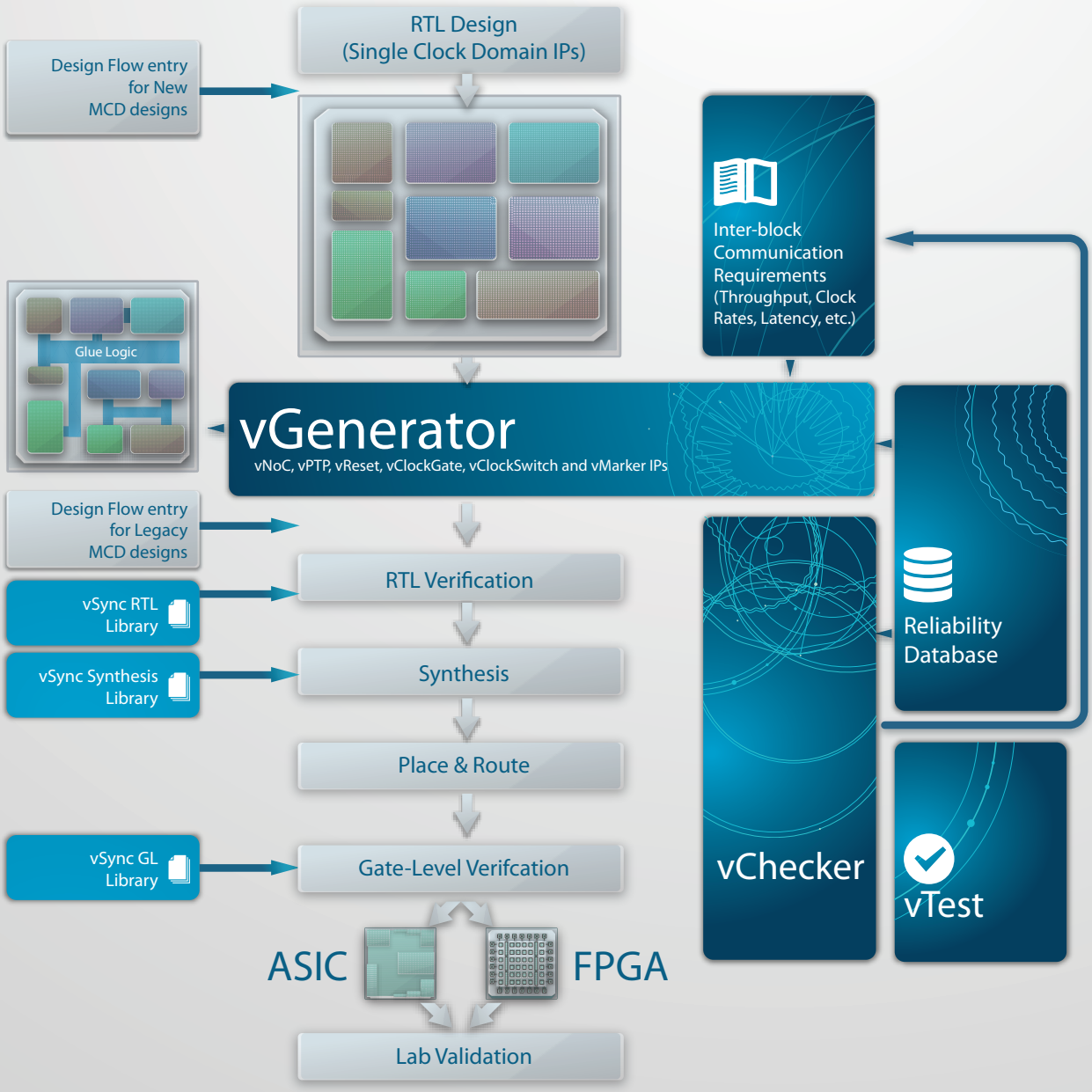
vSync CDC Design and Verification Flow



Synchronization failures are a common pitfall in multiple clock domain designs. These bugs are hard to fix, because the failures are often intermittent and hard to catch. Fixing such bugs in FPGA may take weeks of debugging, and they may be impossible to catch in ASIC prior to fabrication.

vSync Circuits Vincent Platform delivers a twofold solution to this problem. The vGenerator tool provides the necessary fool-proof synchronizer customized for each interface and each clock domain crossing. The vChecker tool verifies the complete design statically, hunting for trouble and assessing expected reliability.

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